CMOS Charge amplifier for liquid argon Time Projection Chamber detectors

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1. INTRODUCTION

We developed an integrated circuit (IC) for the readout of LAr (Liquid Argon) TPC (Time Projection Chamber) neutrino detectors. These detectors employ LAr simultaneously as massive target and detection medium. The detection of secondary particles produced in neutrino interactions is achieved by collecting, on a system of wires at the sides of the detector, the electric charges from the ionization losses. This is obtained by drifting at constant speed the electrons with a high intensity electric field. Two planar coordinates are measured by the wires geometry, the third, perpendicular, coordinate is obtained by measuring the drift time. Typical signals are around 3 fC per particle per wire but they can go up to 120fC. They necessitate of low noise electronics for the readout. The goal is to achieve 1000e- ***ENC (Equivalent Noise Charge)*** with a detector capacitance of 250pF. The distribution of charges collected by the wires is then representative of a 3D image of the tracks of the secondary particles from the neutrino interaction. Normally the readout electronics for these detectors is located externally to the cryostat, implying the use of long flat cables to bring outside the signals collected by the wires. In order to limit cable capacitances (and therefore the noise), we studied the possibility to install the front-end electronics into the Argon vapours, above the LAr filled volume. Argon is liquid between 83 K and 87 K. A typical temperature around 120K is reached in the Argon vapours. Such environment may further improve the electronic noise which decreases with temperature. However, the circuit should dissipate as little heat as possible to prevent additional warming of the detector. The requested characteristics of the circuit are: capability of working at low temperatures, low noise, low heat dissipation, high reliability, low cost. In order to optimize the cost per channel ratio we selected a standard 0.35µ CMOS technology: ***AMSC35B4***.

2. ENVIRONMENT CONTEXT

The 'spectre' simulator used to predict the behaviour of the circuit allows simulating at temperatures down to -250°C, but not beneath -250°C. Yet, as specified in the process parameters document, the process is qualified in the temperature range -40°C <= Tj <= 125°C, where Tj is the transistor junction temperature. The temperature dependent parameters are extracted in the temperature range 25°C < Tj < 125°C. The provided 'SPICE' models are valid in the temperature range -40°C < Tj < 180°C. Thus, there are no warranties on the simulated behaviour underneath -40°C, it is just coming from a mathematical extrapolation. We have then considered the results of the simulations just as first order guidelines and started a systematic campaign to qualify the components and compare, as a function of the temperature, the DC levels and the noise values to real measurements.

3. IMPLEMENTED DESIGN

We started with the characterization of a previous existing circuit [1] built for another application at room temperature but with the same technology. This circuit was oscillating when tested in LN (Liquid Nitrogen). This led us to pay particular attention to the phase margin of our newly designed circuit. We included into the first version of our chip three identical preamplifiers (see on Fig. 1) with a different feedback loop (two different integration time constants and a fully capacitive integrator). We also added some isolated elements for temperature characterization of the resistors and of the transistor threshold voltage Vth.

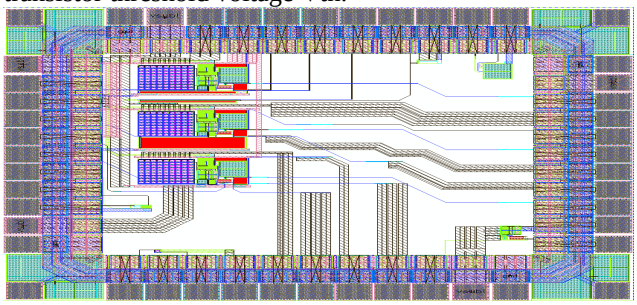

Fig. 1: layout

4. CIRCUIT DESCRIPTION

The general purpose of the circuit is to measure the amount of charge at the input of the system and the time of the charge pulse. Since a pure integrator will saturate after several pulses, a resistance R_{pa} in parallel to the capacitance C_{pa} is needed, see Fig. 2, in order to discharge the integration capacitance C_{pa}.

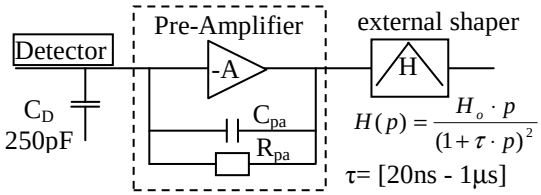

Fig. 2 : simplified setup schematic

The resistance R_{pa} needs to be large enough in order to avoid ballistic effects that would reduce the measured signal. The integration of 2MΩ or 20MΩ resistances in the chosen technology can be achieved with rpolyhc resistances within a reasonable size. “rpolyhc” stand for “Resistance of High Resistive POLYsilicium with parasitic Capacitance model”. The temperature effect on resistance is given in the documentation as a second order equation, see (1). Using a QuadTech 7600 RLC meter, we extracted from measurements the temperature coefficients (RT0, TCR1, TCR2), through bounding and pad, of the integrated 350Ω rpoly2 (R10 on Fig. 3) and 2MΩ rpolyhc resistances. See Table 1.

$$\frac{R(T)}{R(T0)} = 1 + TCR1(T - T0) + TRC2(T - T0)^2 \qquad (1)$$

T0	RT0		TCR1 ($10^{-3}\Omega$/K)	TCR2 ($10^{-6}\Omega$/K)
27°C	spec.	exp	exp	exp
rpoly2	350Ω	400Ω	0.70	1.17
rpolyhc	2MΩ	1.8MΩ	-2.37	5.70

Table 1 : specification vs experimental resistance coeff.

The coefficients experimentally measured in the range [-196; +30°C] are similar to the specification coefficients (not stated here) in the modelling temperature range validity: [-40; +180°C]. Furthermore, we measured the threshold voltage of a PMOS transistor (see left) with parameters Wtot=100µ, L=0.35µ and ngate=10. Since the measured values are close to the theoretical ones given by the simulator, we are now confident that the behaviour of the circuit can be predicted also in the temperature range [-200;-40°C].

temp (°C)	-196	-75	+25
Vth_exp	1.183	0.922	0.733
Vth_th	1.133	0.911	0.731

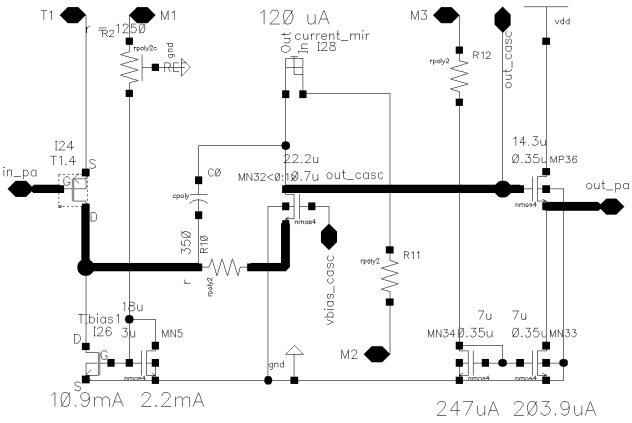

Fig. 3 : Pre-Amplifier schematic

The temperature variation of the DC voltage V_{GS} of the input transistor T1.4 on Fig. 3 was also successfully checked. The biasing circuitry was designed in order to naturally drive more current when cooled down. Together with the phase margin compensation of [2] with C0 and R10 on Fig. 3 and the current increase, the phase margin stayed relatively stable in the studied temperature range. The pre-amplifier integration capacitance C_{pa} connected between "in_pa" and "out_casc" had been set to 0.5pF. Our major issue was the input detector capacitance C_D, to be compared to C_{pa} as an input equivalent capacitance (Fig. 4). C_D has to be negligible with respect to Cpa*A, where A is the Gain of our circuit (75dB@+25°C, 79dB@-196°C), in order to integrate the input charges properly.

5. NOISE PREFORMANCE

The aim of 1000 e^- ENC while expecting a signal of 18 000 e^-, had to be reached for a temperature of -150°C. There are many ways of measuring the ENC such as explained in [3]. But since $V_{out} = K_{pa}.Q_{in}$ and $V_{noise} = K_{pa}.Q_{noise}$, where K_{pa} is the global gain, we considered the measurement of ENC as given in Equation (2). The major electronic voltage noise contribution often labelled as "en" was measured, in absence of input signal, at the output of the system with the 'sdev' (standard deviation) functionality of our oscilloscope. The V_{out} value was measured with the function 'max'. Tests were carried out with or without 1µs shaping on the channel R_{pa} = 2MΩ and R_{pa} = 20MΩ and are shown in Table 2 with a comparison to the theoretical values obtained by simulation.

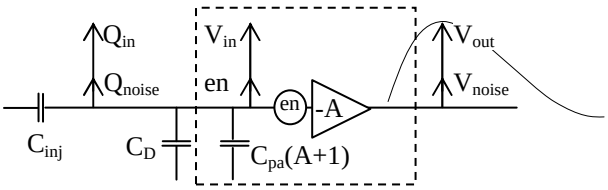

Fig. 4 : Noise test equivalent schematic

$$ENC = \frac{Q_{noise}}{q} = \frac{Q_{in}V_{noise}}{qV_{out}} \qquad (2)$$

Due to higher input impedance, the pure integrator channel is more sensitive to noise from power supply. By powering this channel with a battery, we pinpointed a lack of power supply noise filtering at low temperature. A reduction of the decoupling capacitances at -196°C would explain why the experimental results in Table 2 are less good than expected.

Chip	R_{pa} = 2MΩ				R_{pa} = 20MΩ			
temp	Pre-amp.		+1µs shaper		Pre-amp.		+1µs shaper	
°C	th	exp	th	exp	th	exp	th	exp
30	2040	2261	1530	1590	2225	2720	1272	1648
-111	1722	1847	1002	1166	1811	2111	887	1171
-196	1145	1990	599	1078	1363	2545	581	1310

Table 2 : theoretical vs experimental ENC summary

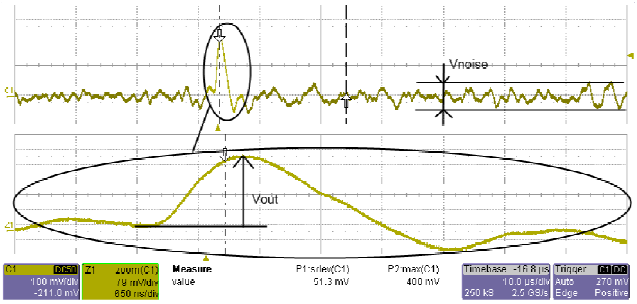

Fig. 5 : 3fC input Charge after 1µs shaper

Fig. 5 represents a typical input signal out of the noise.

6. SUMMARY AND CONCLUSION

This prototype version of the ASIC Pre-Amplifier, produced in June 2007, was fully satisfactory with respect to our goals and allowed us to understand and master the behaviour of these circuits at cryogenic temperature. The results will be presented at this conference. A new produced circuit which consists in a fully integrated multichannel version of the ASIC with preamplifiers, shapers, line buffers and further improvements will be tested soon.

7. REFERENCES

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[2] W. Sansen, Feedforward compensation techniques for high-frequency CMOS amplifiers

[3] D.V. Camin, C.F. Colombo, V.Grassi and G. Pessina, A cryogenic charge-sensitive preamplifier based on the "super-fet" structure, WOLTE4